REMARKS

This is a full and timely response to the Office Action mailed Jun. 14, 2005. Reconsideration and allowance of the application and presently pending claims are respectfully requested.

1.Present Status of the Application

Upon entry of the amendments in this response, claims 242-244 remain pending in the present application. More specifically, claims 242-244 are newly added; and claims 1-241 are canceled without prejudice, waiver, or disclaimer. These additions are specifically described above. It is believed that the foregoing additions add no new matter to the present application.

2.Response To Objections/Rejections

Applicants respectfully traverse the rejections for at least the reasons set forth below.

Response To Claim 242

As originally recited, independent claim 242 recites below:

242. A chip packaging method comprising:
joining a die and a substrate;
after said joining said die and said substrate, depositing a passive device over said substrate; and
separating said substrate.

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Applicants teach the concept that the chip packaging method claimed in claim 242 patentably distinguishes over the citations by Towle et al.

Towle et al. teaches that a chip packaging method comprises joining a die 214 or 314 and a substrate 202 or 302; and separating the substrate 202 or 302. ~ *See FIGS. 11-19 and 32-34 and Pars. [0034] and [0047]* ~ Towle et al. teaches that after joining the die 214 or 314 and the substrate 202 or 302, multiple metal layers 120 and an insulating layer are deposited over the substrate 202 or 302. The insulating layer is deposited between neighboring two of the multiple metal layers 120. ~ *See FIGS. 16 and 34* ~ Towle et al. fails to teach, hint or suggest that the structure of the insulating layer between neighboring two of the multiple metal layers 120 can be formed for a capacitor, but Examiner considers that the structure can be deemed as a capacitor. ~ *See last paragraph of page 3 in the Office Action mailed Jun. 14, 2005* ~ *Applicants disagree with Examiner's perspective because those skilled in the art should think the insulating layer is principally used to electrically insulate the two metal layers 120 if the insulating layer is not particularly stated to be used for a dielectric layer of a capacitor.* Therefore, Towle et al. fails to teach, hint or suggest that a passive device may be formed over the substrate 202 or 302 after joining the die 214 or 314 and the substrate 202 or 302, which is claimed in claim 242.

For at least the foregoing reasons, Applicant respectfully submits that the independent claim 242 patently distinguishes over the prior art references, and should be allowed.

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Response To Claim 243

As originally recited, independent claim 243 recites below:

243. A chip packaging method comprising:
joining a die and a substrate, said die having a top surface at a horizontal level;
after said joining said die and said substrate, depositing a passive device over said horizontal level; and
separating said substrate.

Applicants teach the concept that the chip packaging method claimed in claim 243 patentably distinguishes over the citations by Towle et al.

Towle et al. teaches that a chip packaging method comprises joining a die 214 or 314 and a substrate 202 or 302, the die 214 or 314 having a top surface at a horizontal level; and separating the substrate 202 or 302. ~ *See FIGS. 11-19 and 32-34 and Pars. [0034] and [0047]* ~ Towle et al. teaches that after joining the die 214 or 314 and the substrate 202 or 302, multiple metal layers 120 and an insulating layer are deposited over the horizontal level. The insulating layer is deposited between neighboring two of the multiple metal layers 120. ~ *See FIGS. 16 and 34* ~ Towle et al. fails to teach, hint or suggest that the structure of the insulating layer between neighboring two of the multiple metal layers 120 can be formed for a capacitor, but Examiner considers that the structure can be deemed as a capacitor. ~ *See last paragraph of page 3 in the Office Action mailed Jun. 14, 2005* ~ *Applicants disagree with Examiner's perspective because those skilled in the art should think the insulating layer is principally used to electrically insulate the two metal layers 120 if the insulating layer is not particularly stated to be used for a dielectric layer of a capacitor.* Therefore, Towle et al. fails to teach, hint or suggest that a

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passive device may be formed over the horizontal level after joining the die 214 or 314 and the substrate 202 or 302, which is claimed in claim 243.

For at least the foregoing reasons, Applicant respectfully submits that the independent claim 243 patently distinguishes over the prior art references, and should be allowed.

Response To Claim 244

As originally recited, independent claim 244 recites below:

244. A chip packaging method comprising:
providing a die having a top surface at a horizontal level;
depositing a passive device over said horizontal level; and
depositing a trace over said die and extending to a place under which said die does not exist.

Applicants teach the concept that the chip packaging method claimed in claim 244 patentably distinguishes over the citations by Towle et al.

Towle et al. teaches that a chip packaging method comprises providing a die 214 or 314 having a top surface at a horizontal level; and depositing a trace 120 over the die 214 or 314 and extending to a place under which the die 214 or 314 does not exist. ~ *See FIGS. 11-19 and 32-34* ~ Towle et al. teaches that multiple metal layers 120 and an insulating layer are deposited over the horizontal level. The insulating layer is deposited between neighboring two of the multiple metal layers 120. ~ *See FIGS. 16 and 34* ~ Towle et al. fails to teach, hint or suggest that the structure of the insulating layer between neighboring two of the multiple metal layers 120 can be formed for a capacitor, but Examiner considers that the structure can be deemed as a capacitor. ~

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See last paragraph of page 3 in the Office Action mailed Jun. 14, 2005 ~ Applicants disagree with Examiner's perspective because those skilled in the art should think the insulating layer is principally used to electrically insulate the two metal layers 120 if the insulating layer is not particularly stated to be used for a dielectric layer of a capacitor. Therefore, Towle et al. fails to teach, hint or suggest that a passive device may be formed over the horizontal level, which is claimed in claim 244.

The chip packaging method claimed in claim 244 is supported in Figs. 6 and 7. Referring to Figs. 6 and 7, the chip packaging method comprises providing a die 620 or 720 having a top surface at a horizontal level; and depositing a passive device 644 over the horizontal level, which is claimed in claim 244.

For at least the foregoing reasons, Applicant respectfully submits that the independent claim 244 patently distinguishes over the prior art references, and should be allowed.

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CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 242-244 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
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